RW-WLAN-HE-Top

Release Note
RW-WLAN-HE-RN
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1 Bug

1.1 [11ax]: in TX, wrong ldpc paramters applied for HE_TB with TRS and LDPC

1.1.1 Description

parameter is correcly concumputed but not assigned to framep2_a[1:0]

1.1.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMTXCORE/txvecdec/verilog/rtl/txvecdec.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMTXCORE/txvecdec/verilog/rtl/txvecdec_ucpu.v

1.2 [AX] Main fsm stops rx_bd too early in case of unsupported frame

1.2.1 Description

Rx vector are set to 0, and no useful information are sent to mac. rx_bd must be stops only after rx_end from mpif.

1.2.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/mfsm/verilog/rtl/mfsm.v

1.3 [11ax MAC HW] HE-TB Response bandwidth is not correct when TRS is received in HE-MU frame with bandwidth greater than the maximum supported bandwidth.

1.3.1 Description

The HE-TB response bandwidth should be the bandwidth of the frame that carries the TRS control subfield, but the HE-TB reponse bandwidth is limited to the maximum supported bandwidth.

1.3.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macControllerRx.v

1.4 [11ax MAC HW] Don't decode a trigger frame in an A-MPDU if a another trigger frame was correctly received in same A-MPDU.

1.4.1 Description

An A-MPDU can contain multiple trigger frames, each trigger frame have same content. When a trigger frame is correctly received in an A-MPDU, others trigger frame in the same A-MPDU should not be treated. If other trigger frame is not received correctly (fcs error), the parameters of the correctly received trigger frame are lost.

1.4.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/frameDecoder.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/rxController.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/triggerDecoder.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/rxControllerFsm.v

1.5 [AX] Missing riu interrupt connection to platform

1.5.1 Description

Will allow to detect CCA time-out.

1.5.2 HW impacts

Modified files:

IPs/HW/TOP11ax/rw_he_top/verilog/rtl/rw_he_top.v

1.6 [11ax MAC HW] RHD unique pattern is not written when previous frame is split in receive buffer and discarded.

1.6.1 Description

in rxListProc, when a frame is received with payload split into the receive buffer, if the frame is discarded just after the payload split, slipPayload flag is not cleared. Then the next received frame is not correctly written into memory, RHD uPattern missing.

1.6.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/dmaEngine/verilog/rtl/rxListProc.v

1.7 [AX] Rework FFT memory order for rxtd FO coarse estimation

1.7.1 Description

In order to let SVD working on H for some more time, it is required to move selected memories 2 and 3, dedicated to rxtd during noFFT mode, to memories 0 and 1. Modifications in fft_memmux are required.

1.7.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/fft/verilog/rtl/fft1024x4_memmux.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/hdm_core/verilog/rtl/hdm_core.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXTD/TDFO/verilog/rtl/TDFOCntrl.v

1.8 [AX] CPE wrapping issue with midamble skip case

1.8.1 Description

CpeWrap must be re-computed after midamble skip update case.

1.8.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/CoarseStoCpe.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/CoarseStoCpeTop.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/FDOffsetTop.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/KalmanFilterSTO.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/StoCpeFilter.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/KalmanFilter.v

1.9 [11ax MAC HW] Carrier sense of HE-TB frame is done too early.

1.9.1 Description

When a trigger frame with "CS Required" field set to '1' is received, the HE-TB response should be send only if the medium is not busy during SIFS after the trigger frame reception. The busy detection is done after the MAC/PHY interface rx_end pulse, which is not correct, CCA can be high after this pulse, depend of the RIU latency. The medium busy detection should be done when the HE-TB response should be transmit (after SIFS).

1.9.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macCSReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macCoreReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macController.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macControllerTx.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macTimerUnit/verilog/rtl/macTimerUnit.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/macCore.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/rwWlanNxMACHW.v

1.10 [AX] hrdata must be set to 0 by default in CRM register

1.10.1 Description

1.10.2 HW impacts

Modified files:

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm_reg.v

1.11 [MACSW][HE] assert in rxl_mpdu_transfer

1.11.1 Description

When using HE hardware, rare assert in rxl_mpdu_transfer can be observed: ASSERT (mpdu_len inf RWNX_MAX_AMSDU_RX). Seen in both fhost and fullmac configuration, when no traffic was ongoing on the V7. It is quite rare and I don't have any particular use case to reproduce it, but I saw it several times the last few months so I

log this ticket. One trace (fullmac) is available here /net/rwlab-srv1/nx_share/rwnx_umh/cevav7-6/2019-11-15-14h26m53.824540788

1.11.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/frameDecoder.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/rxController.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/rxControllerFsm.v

1.12 [11ax]: rw_he_crm for all features

1.12.1 Description

1.12.2 HW impacts

Modified files:

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm.v

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm_reset.v

IPs/HW/TOP11ax/rw_he_top/verilog/rtl/rw_he_top_wrapper.v

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm_clock_gate.v

1.13 [11ax MAC HW] A-MPDU delimiter of an BFR Frame sent in HE-TB format is not correct.

1.13.1 Description

When a beamforming report is sent in HE-TB format, an HT Control field with UPH control is added to the BFR frame. The length in the A-MPDU delimiter of the BFR frame doesn't include this extra field (HT Control) which generate error on the receiver side.

1.13.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macControllerRx.v

1.14 [11ax HDMCORE]:BFMEE memory has a persistent content and shall not be shared

1.14.1 Description

currently shared with FD/BD for BCC row fifo and LDPC fifo. if the beamforming report poll request frame or a BFRP trigger frame is any of the HT,VHT or HE format, the bfmee content is destroyed during the receive.

1.14.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/hdm_core/verilog/rtl/hdm_core.v

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm.v

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm_clock_gate.v

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm_clock_generation.v

IPs/HW/TOP11ax/rw_he_memories/verilog/rtl/rw_he_memories.v

IPs/HW/TOP11ax/rw_he_top/verilog/rtl/rw_he_top.v

IPs/HW/TOP11ax/rw_he_top/verilog/rtl/rw_he_top_wrapper.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/bdfd_memmux/verilog/rtl/bdfd_memmux.v

1.15 [11ax]: txvecdec_ucpu/tx_scheduler do not treat nsym=0 as inconsistent

1.15.1 Description

Occurs if the AP returns inconsitent parameters in the trigger frame common field.

1.15.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMTXCORE/tx_scheduler/verilog/rtl/tx_scheduler.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMTXCORE/txvecdec/verilog/rtl/txvecdec_ucpu.v

1.16 [11ax MAC] Wrong computation of TXOPDuration

1.16.1 Description

When running WiFi-Alliance testing, a check on the computed TXOPDuration carried in the HE-SIGA of the HE_TB failed. After analysis, the macController does not compute correctly the duration of the HE_TB. In the current implementation, the HE_TB frame duration is computed using HE parameters (MCS/aMPDU Length/Preamble type/...) of the HE_TB. The correct computation shall be done using the extracted UL Length, a legacy preamble and a datarate of 6Mbps.

1.16.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macControllerRx.v

1.17 [11ax]: txvecdec_upcu, missing operation for nma computation

1.17.1 Description

1.17.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMTXCORE/txvecdec/verilog/rtl/txvecdec.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMTXCORE/txvecdec/verilog/rtl/txvecdec_ucpu.v

1.18 [11ax]: bd_rx_ctrl_ucpu, missing operation for nma computation

1.18.1 Description

o like txvecdec_ucpu, needs a review

1.18.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMTXCORE/txvecdec/verilog/rtl/txvecdec_ucpu.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXBD/rx_bd_ctrl/verilog/rtl/rx_bd_ctrl_ucpu.v

1.19 [AX] Missing unsupported frame for STA20 only receiving a HE MU RU242

1.19.1 Description

1.19.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXBD/rx_bd_ctrl/verilog/rtl/rx_bd_ctrl_rxvector.v

1.20 [11ax] transmit power of the HE-TB Frame sent in response to a frame with TRS control field is not correct.

1.20.1 Description

The TRS control field contain information for the transmit power of the HE-TB response frame, but the maximum transmit power is used instead of the expected transmit power, computed from the TRS parameters.

1.20.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/txController/verilog/rtl/txVectorSel.v

1.21 [11ax MAC HW] Intra-BSS and inter-BSS PPDU classification has changed in 802.11ax Draft 4.0

1.21.1 Description

The inter-BSS and intra-BSS PPDU classification has changed in 802.11ax Draft 4.0 specification, but the MAC HW has not been updated accordingly.

1.21.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/rxControllerFsm.v

1.22 [HOST DMA] The AXI error response is not correctly handled by the host DMA downstream interface.

1.22.1 Description

In case of error response from the AXI interface, the downstream interface stop the exchange and clear the read context of the exchange. In case of error response from the AXI interface on first data, the downstream r_state is stuck into the R_INIT state until a data is provided without error response. In case of error response from the AXI

interface, the downstream should accept all expected data, which are probably corrupted, and then close the transfert with an ERROR interrupt.

1.22.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/rw_host_dma/verilog/rtl/dma_ctrl.v

IPs/HW/TOP11ax/MACSUBSYS/rw_host_dma/verilog/rtl/downstream_axi.v

1.23 [AX] FDO estimation on 20MHz secondary for HESIGB offset tracking

1.23.1 Description

1.23.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXTD/RxTDTop/verilog/rtl/RxTDTop.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/ofdm_rx_core/verilog/rtl/ofdm_rx_core.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXTD/RxTDTop/verilog/rtl/RxTimeDomainStMc.v

1.24 [AX] VHT/HE first byte rxvector must be sent as soon as VHT/HE SIGA is decoded and qualified.

1.24.1 Description

1.24.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMTXCORE/ofdm_tx_core/verilog/rtl/ofdm_tx_core.v

1.25 [11ax MAC HW] TSF field of the RHD is incorrect when rxEndForTiming pulse is received before the end of receive vector.

1.25.1 Description

The rxEndForTiming pulse can be received during the receive vector reception. In this case, the TSF field of the Receive Header Descriptor is null.

1.25.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/rxController.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/rxFIFOIfController.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/rxControllerFsm.v

2 Feature

2.1 [AX] HEMU80 not supported with NON-AP STA20M only

2.1.1 Description

2.1.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXBD/rx_bd_ctrl/verilog/rtl/rx_bd_ctrl_rxvector.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/ChEstSmth/verilog/rtl/ChEstSmthTop.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/ChEstSmth/verilog/rtl/EstimController.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/ChEstSmth/verilog/rtl/EstimRotCtrl.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/ChEstSmth/verilog/rtl/EstimSmoothRx.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/ChEstSmth/verilog/rtl/EstimSmoothStream.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/ChEstSmth/verilog/rtl/FilterCoeffSelect.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/ChEstSmth/verilog/rtl/PilotAveraging.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/ChEstSmth/verilog/rtl/SmoothTop.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/CoarseStoCpe.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/CoarseStoCpeTop.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/FDOComp.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/FDOffsetTop.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/KMulGamma.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/MNMatrix.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/RefPhase.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/FDOffset/verilog/rtl/WLSCoefCompTop.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/RxFDTop/verilog/rtl/RxFDTop.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/RxFDTop/verilog/rtl/RxFreqDomainStMc.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/equalizer_rx1_ss1/verilog/rtl/EqualizerRX1SS1.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/equalizer_rx1_ss1/verilog/rtl/equalizer_fddc.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/equalizer_rx1_ss1/verilog/rtl/equalizer_genindex.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXTD/RxTDTop/verilog/rtl/RxTimeDomainStMc.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/ofdm_rx_core/verilog/rtl/ofdm_rx_core.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/hdm_core/verilog/rtl/hdm_core.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXFD/ChEstSmth/verilog/rtl/HWriteCtrl.v

2.2 [11ax MAC HW] Add support of A-MPDU transmission with QoS-Null frames.

2.2.1 Description

MAC HW Should support the transmission of A-MPDU frames with QoS-Null frames. This is needed for BSRP trigger frame response.

2.2.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/txController/verilog/rtl/formatMPDU.v

2.3 [AX] RIU not supporting HE-MU format for gain update in HE-STF

2.3.1 Description

2.3.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/ofdm_rx_core/verilog/rtl/ofdm_rx_core.v

IPs/HW/TOP11ax/PHYSUBSYS/MDMCOMMON/RIUCORE/AGC/AGCFSM/verilog/rtl/RFGainSet.v

IPs/HW/TOP11ax/PHYSUBSYS/MDMCOMMON/RIUCORE/IQIMBALANCE/iq_est/verilog/rtl/iq_est_ctrl.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXTD/RxTDTop/verilog/rtl/RxTimeDomainStMc.v

2.4 [11ax MAC HW] All supported type of frames should be supported in TX in MPDU, S-MPDU or A-MPDU.

2.4.1 Description

Update the txController to support same type of frames in an A-MPDU, as it is supported in MPDU or S-MPDU. For example, a frame without frame body.

2.4.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/txController/verilog/rtl/formatMPDU.v

2.5 [11ax MAC HW] Add possibility to halt TB DMA Channel.

2.5.1 Description

2.5.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macCSReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macPIReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/rwWlanNxMACHW.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/dmaEngine/verilog/rtl/dmaEngineWrapper.v

2.6 [11ax]: TXCORE CMAP coefficient resizing

2.6.1 Description

2.6.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMTXCORE/tx_fd_cmap/verilog/rtl/tx_fd_cmap.v

2.7 [11ax MAC HW] Add possibility to disable the HE-TB response in RU26.

2.7.1 Description

When requested by SW, the MAC HW should disable the HE_TB response if the allocated RU is a 26-tones RU.

2.7.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macCSReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macCoreReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macController.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/macCore.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/rwWlanNxMACHW.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macControllerRx.v

2.8 [11ax MAC HW] Add possibility to send block-ack frame in response of a basic Trigger frame.

2.8.1 Description

When a basic trigger frame is received inside an A-MPDU and this A-MPDU contain an MPDU which need an HTP Ack response, the HE-TB response frame should contain a ack or block-ack frame. # Ack/Block-ack is generated by SW and provided to HW. # Ack/Block-ack is generated by SW with empty block-ack bitmap and provided to HW. HW will update block-ack bitmap on transmission. # Ack/Block-ack is generated by HW. 3rd solution implemented.

2.8.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rxController/verilog/rtl/frameDecoder.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macControllerRx.v

2.9 [11ax MAC HW] Add possibility to process beamforming report with active reception.

2.9.1 Description

When receive a calibration procedure (NDP-A + NDP), the reception is stopped during the SVD processing in order to prevent memory corruption. For debug purpose, we should be able to have the reception active during the SVD processing.

2.9.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macCSReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macCoreReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macController.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/macCore.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/rwWlanNxMACHW.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macControllerMaster.v

2.10 [11ax MAC HW] Compute and provide to SW the PSDU Length of the HE-TB frame.

2.10.1 Description

When a trigger frame is received and a HE-TB response is expected, the PSDU length available in the HE-TB response should be computed and provided to SW.

2.10.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macCSReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/macCore.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/rwWlanNxMACHW.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/tbCalculator/verilog/rtl/tbCalculator.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macPlReg.v

2.11 [11ax MAC HW] Provide "AP TX POWER" and "UL TARGET RSSI" fields of the received trigger frame to SW.

2.11.1 Description

The "AP TX POWER" field of the common info field and "UL TARGET RSSI" field of the user info field are needed to compute the UPH Control field of the trigger based response. the MAC HW can provide these 2 fields to software with the computed UPH control field.

2.11.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macCSReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macCSReg/verilog/rtl/macPlReg.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macController.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/macCore.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/rwWlanNxMACHW/verilog/rtl/rwWlanNxMACHW.v

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/macController/verilog/rtl/macControllerRx.v

2.12 [11ax]: bdfd_memmux, add support for single or double cycle bfmee interface

2.12.1 Description

2.12.2 HW impacts

Modified files:

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm.v

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm_clock_generation.v

IPs/HW/TOP11ax/rw_he_crm/verilog/rtl/rw_he_crm_fpga.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/BFCORE/bfr_mpif/verilog/rtl/bfr_mpif.v

2.13 rx_bd_ctrl_ucpu: o replaced verilog include by source codeofdm_rx_bd: o initial revision o added missing .list filesviterbi: o imported from 11ac branch

2.13.1 Description

2.13.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXBD/rx_bd_viterbi/verilog/rtl/rx_bd_viterbi.v

2.14 Copy previous svn history from old version hierarchy

2.14.1 Description

2.14.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXBD/rx_bd_viterbi/verilog/rtl/rx_bd_viterbi.v

2.15 [11ax RTL] added missing define for max pilot value set to 6

2.15.1 Description

2.15.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/cfg/hdm_core_config.v

2.16 [11ax]: lint

2.16.1 Description

2.16.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/MACCORE/tbCalculator/verilog/rtl/tbCalculator.v

2.17 [AX] OFDM RX BD integration

2.17.1 Description

2.17.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXBD/rx_bd_viterbi/verilog/rtl/rx_bd_viterbi.v

2.18 [11ax] Add debug port

2.18.1 Description

Add new diag port

2.18.2 HW impacts

Modified files:

IPs/HW/TOP11ax/MACSUBSYS/rw_host_dma/verilog/rtl/downstream_axi.v

IPs/HW/TOP11ax/MACSUBSYS/rw_host_dma/verilog/rtl/downstream_channel.v

IPs/HW/TOP11ax/MACSUBSYS/rw_host_dma/verilog/rtl/rw_host_dma.v

IPs/HW/TOP11ax/MACSUBSYS/rw_nx_platform/verilog/rtl/rw_nx_platform.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXBD/ofdm_rx_bd/verilog/rtl/ofdm_rx_bd.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXBD/rx_bd_ctrl/verilog/rtl/rx_bd_ctrl.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/ofdm_rx_core/verilog/rtl/ofdm_rx_core.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/hdm_core/verilog/rtl/hdm_core.v

IPs/HW/TOP11ax/rw_he_top/verilog/rtl/rw_he_top.v

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/OFDMACORE/OFDMRXCORE/OFDMRXBD/rx_bd_ctrl/verilog/rtl/rx_bd_ctrl_fsm.v

2.19 [AX] Add Diag Port on hdm_core

2.19.1 Description

2.19.2 HW impacts

Modified files:

IPs/HW/TOP11ax/PHYSUBSYS/HDMCORE/hdm_core/verilog/rtl/hdm_core.v